(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 411 612 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **90114775.1**

(51) Int. Cl.5: **H01L 33/00**

(22) Date of filing: **01.08.90**

(30) Priority: **02.08.89 JP 200481/89**
04.08.89 JP 203055/89

(43) Date of publication of application:
06.02.91 Bulletin 91/06

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **CANON KABUSHIKI KAISHA**
30-2, 3-chome, Shimomaruko, Ohta-ku
Tokyo(JP)

(72) Inventor: **Tsukamoto, Takeo c/o Canon**
Kabushiki Kaisha
30-2, 3-chome Shimomaruko
Ohta-ku, tokyo(JP)
Inventor: **Okunuki, Masahiko, c/o Canon**
Kabushiki Kaisha
30-2, 3-chome, Shimomaruko
Ohta-ku, Tokyo(JP)
Inventor: **The other inventors have agreed to waive their entitlement to designation**

(74) Representative: **Pellmann, Hans-Bernd,**
Dipl.-Ing. et al
Patentanwaltsbüro
Tiedtke-Bühling-Kinne-Grupe-Pellmann-Grams-Struif Bavariaring 4
D-8000 München 2(DE)

(54) Semiconductor light-emitting device.

(57) A semiconductor light emitting device comprises a substrate, an n-type semiconductor layer formed on the substrate, a p-type semiconductor layer formed on a portion of a surface of the n-type semiconductor layer, an electrode for applying a reverse biasing voltage to the PN junction to cause an avalanche breakdown and an area formed in a portion of the PN junction. The p-type semiconductor layers forms a planar type PN junction with the n-type semiconductor layer. The area formed in a portion of the PN junction has a lower break down voltage than that of other area.

FIG. 1A

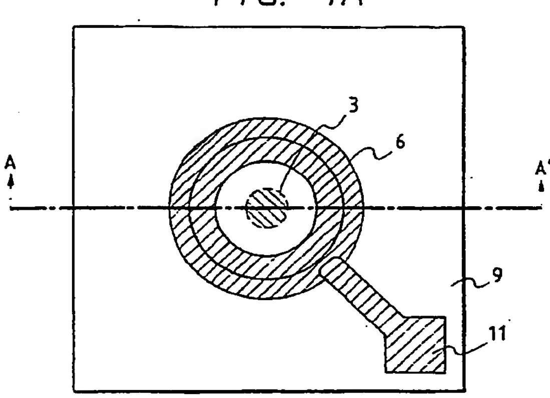
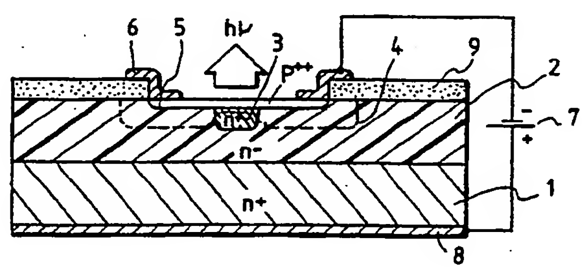


FIG. 1B



EP 0 411 612 A2

SEMICONDUCTOR LIGHT-EMITTING DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor light-emitting device which has a planar type PN junction or a Schottky junction and produces a light by applying a reverse bias to the junction to cause an avalanche breakdown.

Related Background Art

Photo-emission from avalanche breakdown has been reported by an article "Photo emission from avalanche breakdown" by A.G. Chynoweth and H.K. Mckey, Phys. Rev., Vol. 102, p.369, 1956. On the other hand, an application of the photo emission phenomenon to a light emitting semiconductor element is reported in "A study of the nature and characteristics of light radiation in reverse-biased silicon junctions" by C.B. Williams and K. Daneshver, Conf. Proc. IEEE, sou theostion, p.161, 1988. In this article, it is reported that a photo emission intensity on a Si PN junction interface is 0.01 W/cm^2. The semiconductor devices in those articles comprise planar type PN junctions as described in "Physics of Semiconductor Devices" by S.M. Sze, John Wiley & Sons, p.73.

In the prior art devices, because of the planar type PN junction, there exists a portion having a cylindrical radius of curvature or spherical radius of curvature around the junction. Since an electric field acting on the junction is higher in the portion having the cylindrical or spherical radius of curvature than in a planar junction portion, the photo emission by the avalanche breakdown occurs only in the high electric field zone, that is, only periphery of the junction, and it is not possible to uniformly emit light throughout the junction. In such a planar junction, there occurs photo emission by an electric field concentration due to ununiformity of a paterning shape in the formation of the junction or photo emission by an electric field concentration due to defects. Thus, photo emission by inadvertent factors governs the light intensity of the photo emission or the position of the photo emission. Accordingly, it is not possible to form a light emitting device with a high control.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor light emitting device which solves the problems encountered in the prior art devices, can be manufactured with a high control and emits light uniformly.

The above object of the present invention is achieved by a semiconductor light emitting device comprising:
a substrate;
an n-type semiconductor layer formed on said substrate;
a p-type semiconductor layer formed on a portion of a surface of said n-type semiconductor layer;
said p-type semiconductor layer forming a planar type PN junction with said n-type semiconductor layer;
an electorde for applying a reverse biasing voltage to said PN junction to cause an avalanche breakdown; and
an area formed in a portion of said PN junction;
said area having a lower breakdown voltage than that of other area.

Further, the above object of the present invention is achieved by a semiconductor light emitting device comprising:
a substrate;
an n-type semiconductor layer formed on said substrate;
a Schottky electrode layer formed on said n-type semiconductor layer;
said Schottky electrode layer forming a Schottky junction with the n-type semiconductor layer;
a contact electrode for applying a reverse biasing voltage to said Schottky junction to cause an avalanche breakdown; and
an area formed in a portion of said Schottky junction;
said area having a lower breakdown voltage than other area.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B show a plan view and a sectional view of a first embodiemnt of a semiconductor light emitting device of the present invention,
Fig. 2 shows an energy band of the device shown in Fig. 1,
Fig. 3 illustrates a light emission process in the device of the present invention,
Fig. 4 shows a relation between a photon energy and a light intensity in the device shown in Fig. 1,
Fig. 5 shows a sectional view of a second embodiment of the present invention,

Figs. 6A and 6B show a plan view and a sectional view of a third embodiment of the present invention,

Fig. 7 shows an energy band of the device shown in Fig. 6, and

Fig. 8 shows a sectional view of a fourth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figs. 1A and 1B show a plan view and an A-A′ sectional view of a first embodiment of the semiconductor light emitting device of the present invention. This device manufactured by the following process.

An n-type semiconductor layer 2 having an impurity concentration of 3×10^{16} cm^{-3} was formed on an n-type semiconductor substrate 1 (GaAs (100) in the present embodiment) by monochrome beam epitaxy (MBE) growth. Photoresist in an area 3 is cut by a photolithography resist process, and Si ions were injected therein at an acceleration voltage of 80 KeV. Further, photoresist in an area 5 was cut by a similar resist process and Zn ions were injected therein at an acceleration voltage of 40 KeV.

It is then annealed in an arsine environment at 850°C for 30 seconds to activate the impurity atoms. The area 3 was rendered to a highly doped n-type area having a peak impurity concentration of approximately 1×10^{18} cm^{-3}, and the area 5 to a p-type semiconductor layer having a peak impurity concentration of no smaller than approximately 1×10^{19} cm^{-3}. The size of the highly doped n-type area 3 is preferably no larger than 5 µm in diameter. When it is larger than 5 µm, a uniform light emission is not attained and heat generation increases. The thickness of the p-type semiconductor layer is preferably no larger than 0.1 µm. If it is larger than 0.1 µm, a light transmittance rapidly decreases.

SiO_2 was sputtered on the semiconductor layer to form an insulation layer 9. Photoresist at a predetermined position was cut by the same resist process as that described above and a portion of the insulation layer 9 was etched off to form an opening. Cr/Au was vapor-deposited thereon and unnecessary portion was removed by etching, and an ohmic contact electrode 6 to the p-type semiconductor was formed. An Aℓ contact electrode 11 was formed to be connected to the electrode 6. An ohmic contact electrode 8 was formed on a bottom surface of the substrate 1. A reverse biasing electric field was applied to the device thus formed from a power supply 7 through electrodes 6 and 8 so that a light $h\nu$ was emitted from the top of the area 3.

The operation of the device of the present invention is now explained.

Fig. 2 shows an energy band of the semiconductor light emitting device of the present invention. As shown in Fig. 2, by jointing the p-type semiconductor layer to the n-type semiconductor layer and applying the reverse bias to cause the avalanche breakdown, a number of electrons and holes are generated in a depletion layer. The generated electrons and holes cause not only a normal inter-band transition shown by a in Fig. 3 but also a recombination of carriers having a high energy shown by b or an intra-band transition shown by c, and the light is emitted.

In the present embodiment, the highly doped n-type area 3 which is distinctive from other area is formed in the n-type semiconductor layer 2 to from a depletion layer shown by a broken line 4 in Fig. 1B. An uniform and high electric field area is formed throughout the highly doped n-type area 3 so that the light emission uniformly occurs only in the highly doped area.

In the present embodiment, by forming the highly doped area, the high electric field is formed to increase an electron-hole pair generation efficiency to increase the light emission probability and attain a brightness control. Further, by applying a high energy to the electrons-holes, a light having a larger energy than a band gap Eg is emitted.

In the present embodiment, the n-type semiconductor is used as the semiconductor substrate. Thus, a highest electric field is formed below the p-type semiconductor which is exposed to the surface, and the electrons which are minority carriers in the p-type semiconductor most act on the avalanche amplification. As a result, where a substrate (for example, silicon) in which the electron-hole pair generation efficiency varies depending on the type of carriers and the probability of generation of the electron-hole pairs by the electron is larger than the probability of generation of the electron-hole pairs by the holes, the electron generation efficiency is improved by the present embodiment.

In the present embodiment, it is necessary that the thickness of the p-type semiconductor layer is very thin enough to fully transmit the light generated at the PN junction interface and reduce a light transmission loss.

By the above arrangement, a light emitting device having a relation between the photon energy and the light intensity as shown in Fig. 4 is manufactured with a high control.

Fig. 5 shows a second embodiment of the present invention. Fig. 5 shows a sectional view of the device as Fig. 1B does. In Fig. 5, the like elements to those shown in Fig. 1B are designated by the like numerals. The device was manufactured

in the following process.

An n-type semiconductor layer 2 having an impurity concentration of 5×10^{16} cm^{-3} was epitaxially grown on an n-type semiconductor substrate (Si (100) in the present embodiment) by a vapor deposition (CVD) method. Then, SiO_2 was formed to a thickness of 4000 Å by thermal diffusion, and resist at a predetermined position was cut by a resist process and SiO_2 was removed by fluodic acid etchant to form a donut-shaped opening on the top of the area 10. Then, B (boron) was thermal-diffused by appropriate dopant to form a p-type guard ring area 10. Then, the SiO_2 area at the top of the light emission area was removed by the resist process and the etchant. P ions (phosphorus) were injected into the area 3 and Ga(galium) ions were injected into the area 5 to make the area 3 to the n-type semiconductor having a peak impurity concentration of approximately 8×10^{17} cm^{-3} and the area 5 to the p-type semiconductor having a peak impurity concentration of no smaller than approximately 1×10^{19}. The ions were injected at a low acceleration so that the thickness of the area 5 is no larger than 500 Å, and it was appropriately etched. Then, ohmic contact electrodes 6 and 8 were formed to complete the light emitting device. In the present embodiment, the guard ring area 10 is formed around the highly doped n-type area 3 to form the depletion layer shown by the broken line 4 so that the electric field is further concentrated to the area 3 to improve the light emission efficiency.

Figs. 6A and 6B show a plan view and an A-A′ sectional view of a third embodiemnt of the semiconductor light emitting device of the present invention. This device was manufactured in the following process.

First, an n-type semiconductor layer 12 having an impurity concentration of 3×10^{15} cm^{-3} was formed on an n-type semiconductor substrate 21 (GaAs (100) in the present embodiemnt) by molecule beam epitaxy (MBE) growth. Photoresist in an area 13 was cut by a photo-lithography resist process, and Si ions were injected therein at an acceleration voltage of 80 KeV. Then, it was annealed in an arsine environment at 850°C for 30 seconds to activate the impurity atoms. The area 13 was rendered to a highly doped semiconductor area having a peak impurity concentration of approximately 1×10^{18} cm^{-3}.

Then, SiO_2 was deposited by a sputtering method to a thickness of 4000 Å, and resist at a predetermined position was cut by the same resist process as that described above. The SiO_2 at a portion of the top of the device was removed by fluodic acid wet etching and an insulation layer 19 was formed. Then, Cr/Au was vapor-deposited and unnecessary portion was removed by etching. An ohmic contact electrode layer 16 was formed to contact to a Schottky electrode 15 to be formed later. An ohmic contact electrode 18 was also formed on the bottom surface of the substrate 21.

W (tangusten) was deposited as a Schottky electrode 15 to a thickness of approximately 150 Å by electron beam (EB) vapor deposition to from a Schottky junction. The n value was 1.05 at a barrier height ϕ_{SB} = 0.8 eV of the Schottky junction. Finally, an Aℓ contact electrode 31 was formed. A reverse biasing electric field was applied to the device thus manufactured from a power supply 17 through electrodes 16 and 18. The light $h\nu$ was emitted from the top of the area 13.

The operation of the device of the present invention is now explained.

Fig. 7 shows an energy band of the semiconductor light emitting device of the present invention. As shown in Fig. 7, the Schottky electrode layer is jointed to the n-type semiconductor layer and the reverse bias is applied thereto to cause the avalanche breakdown so that a number of electrons and holes are generated in the depletion layers. The generated electrons and holes causes the inter-band transition, carrier recombination or intra-band transition as shown in Fig. 3 to emit a light.

In the present embodiment, the highly doped n-type area 13 which is distinctive from other area is formed in the n-type semiconductor layer 12 to form the depletion layer as shown by the broken line 14 in Fig. 6B. By forming a uniform and high electric field area throughout the highly doped n-type area 13, the light emission occurs uniformly only in the highly doped area.

In the present embodiment, the highly doped area is formed as described above to form the high electric field and increase the electron-hole pair generation efficiency and increase the probability of light emission in order to attain the brightness control. Further, a large energy is applied to the electrons-holes so that a light having a larger energy than the band gap Eg is emitted.

In the present embodiment, the n-type semiconductor is used as the semiconductor substrate. Thus, the highest electric field is formed below the Schottky electrode on the surface and the electrons in the Schottky electrode most act on the avalanche amplification. Accordingly, where the substrate (for example, silicon) in which the electron-hole pair generation efficiency varies depending on the type of carrier and the probability of generation of the electron-hole pairs by the electrons is larger than the probability of generation of the electron-hole pairs by the holes, the electron generation efficiency is improved by the present embodiment.

In the present embodiment, it is necessary that the thickness of the Schottky electrode layer be very thin enough to fully transmit the light generated at the PN junction interface and reduce the

light transmission loss. In this connection, the thickness of the electrode layer is preferably no longer than 0.1 μm. In the present embodiment, a relation between the photon energy and the light intensity is same as that shown in Fig. 4 for the first embodiment.

Fig. 8 shows a fourth embodiment of the present invention. Fig. 8 shows a sectional view of the device as Fig. 6B does. In Fig. 8, the like elements to those shown in Fig. 6B are designated by the like numerals. This device was manufactured by the following process.

First, an n-type semiconductor layer 12 having an impurity concentration of 5×10^{16} cm^{-3} was epitaxially grown on an n-type semiconductor substrate 21 (Si (100) in the present embodiment) by a vapor deposition (CVD) method. Then, SiO_2 was formed to a thickness of 4000 Å by thermal diffusion. Resist at a predetermined position was cut by the resist process, and the SiO_2 at that position was removed by fluodic acid etchant to form a donut-shaped opening on an area 30. Then, B (boron) was thermal-diffused by appropriate dopant to form a p-type guard ring area 30. The SiO_2 at the top of the light emission area was removed by the above-mentioned resist process and etchant, and P (phosphorus) ions were injected in an area 13 in the same manner as that of the third embodiment to form the n-type semiconductor having a peak impurity concentration of approximately 8×10^{17} cm^{-3} after annealing. Then, ohmic contact electrodes 16 and 18 were formed, and finally Au was vapor-deposited to a thickness of 150 Å to form a Schottky electrode 15.

In the present embodiment, Au is used as the material of the Schottky electrode although it is not restrictive and any other material which forms a Schottky junction may be used. A material other than metal such as silicide, carbonide or boronide may be used. A material which has a low resistivity, a high light transmittance and exhibits uniformity even if it is thin is preferable.

In the present embodiment, the guard ring area is formed around the highly doped n-type area 13 to form the depletion layer shown by the broken line 14 and the electric field is concentrated thereto. Accordingly, the light emission efficiency is improved.

The present invention nay be applicable in various forms other than the above embodiments. The present invention covers all such modifications without departing from the scope of claims.

A semiconductor light emitting device comprises a substrate, an n-type semiconductor layer formed on the substrate, a p-type semiconductor layer formed on a portion of a surface of the n-type semiconductor layer, an electrode for applying a reverse biasing voltage to the PN junction to cause an avalanche breakdown and an area formed in a portion of the PN junction. The p-type semiconductor layers forms a planar type PN junction with the n-type semiconductor layer. The area formed in a portion of the PN junction has a lower break down voltage than that of other area.

Claims

1. A semiconductor light emitting device comprising:
a substrate;
an n-type semiconductor layer formed on said substrate;
a p-type semiconductor layer formed on a portion of a surface of said n-type semiconductor layer;
said p-type semiconductor layer forming a planar type PN junction with said n-type semiconductor layer;
an electrode for applying a reverse biasing voltage to said PN junction to cause an avalanche breakdown; and
an area formed in a portion of said PN junction;
said area having a lower breakdown voltage than that of other area.

2. A semiconductor light emitting device according to Claim 1 wherein said area having the lower breakdown voltage is formed by forming a higher impurity concentration portion than other portion in a portion of the n-type semiconductor layer adjoining to the p-type semiconductor layer.

3. A semiconductor light emitting device according to Claim 1 wherein the P-type semiconductor layer around the lower breakdown voltage area is thicker than other portion of the p-type semiconductor layer.

4. A semiconductor light emitting device according to Claim 1 wherein the size of the lower breakdown voltage area is no larger than 5 μm.

5. A semiconductor light emitting device according to Claim 1 wherein the thickness of the p-type semiconductor layer in the lower breakdown voltage area is no larger than 0.1 μm.

6. A semiconductor light emitting device comprising:
a substrate;
an n-type semiconductor layer formed on said substrate;
a Schottky electrode layer formed on said n-type semiconductor layer;
said Schottky electrode layer forming a Schottky junction with the n-type semiconductor layer;
a contact electrode for applying a reverse biasing voltage to said Schottky junction to cause an avalanche breakdown; and
an area formed in a portion of said Schottky junction;

said area having a lower breakdown voltage than other area.

7. A semiconductor light emitting device according to Claim 6 wherein said lower breakdown voltage area is formed by forming a portion having a higher impurity concentration than other area in a portion of the n-type semiconductor layer adjoining to the Schottky junction.

8. A semiconductor light emitting device according to Claim 6 further comprising a ring-shaped p-type semiconductor layer formed around the lower breakdown voltage area.

9. A semiconductor light emitting device according to Claim 6 wherein the size of said lower breakdown voltage area is no larger than 5 μm.

10. A semiconductor light emitting device according to Claim 6 wherein the thickness of the Schottky electrode layer in the lower breakdown voltage area is no larger than 0.1 μm.

FIG. 1A

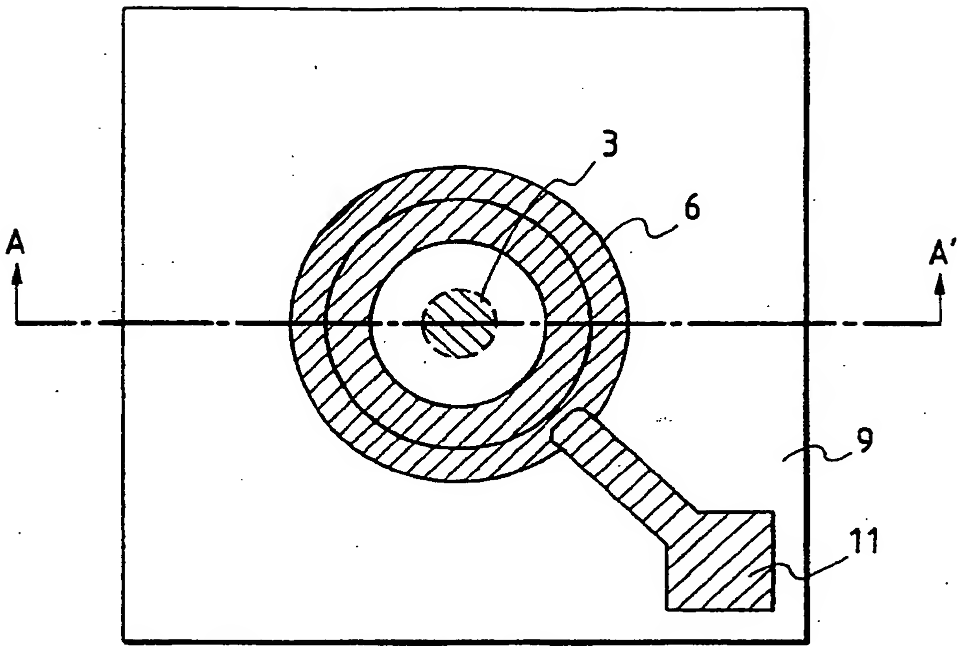
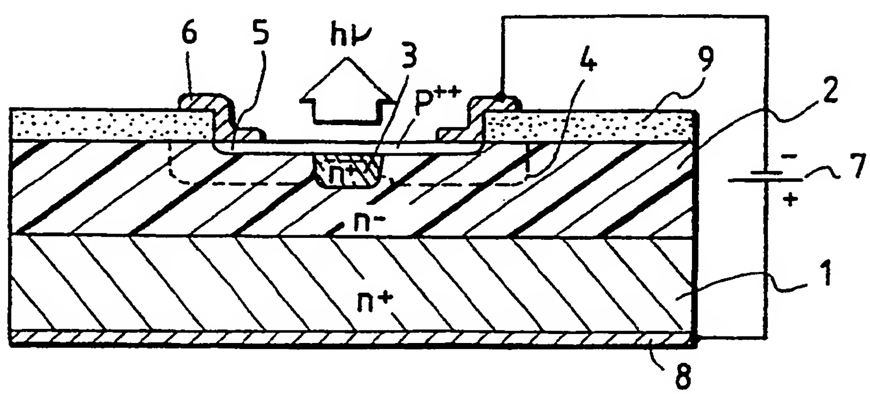


FIG. 1B



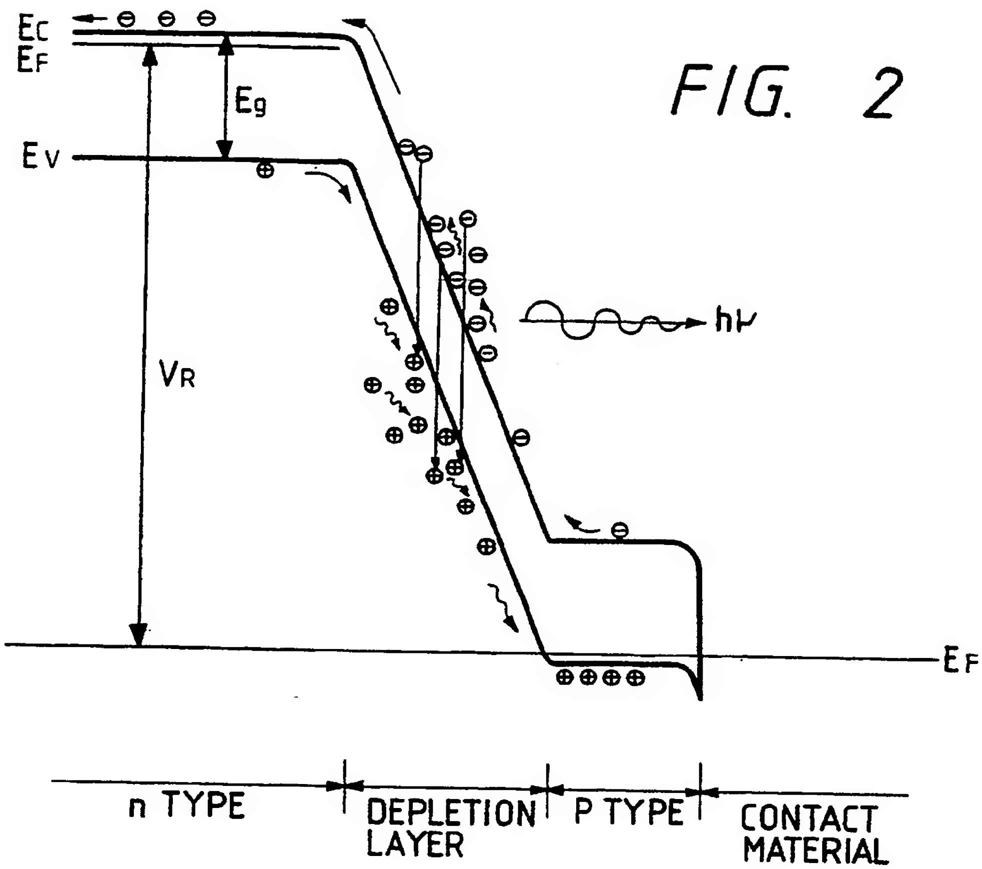

EC
EF
Eg
EV
VR
hν
EF
n TYPE
DEPLETION LAYER
P TYPE
CONTACT MATERIAL

FIG. 2

FIG. 3

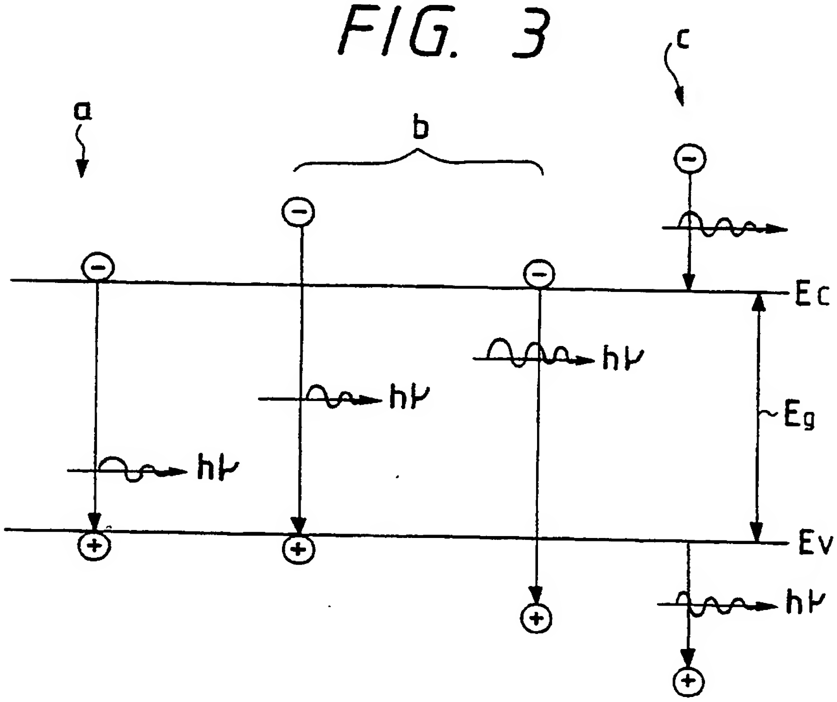

a
b
c
hν
hν
hν
Ec
Eg
Ev
hν

FIG. 4

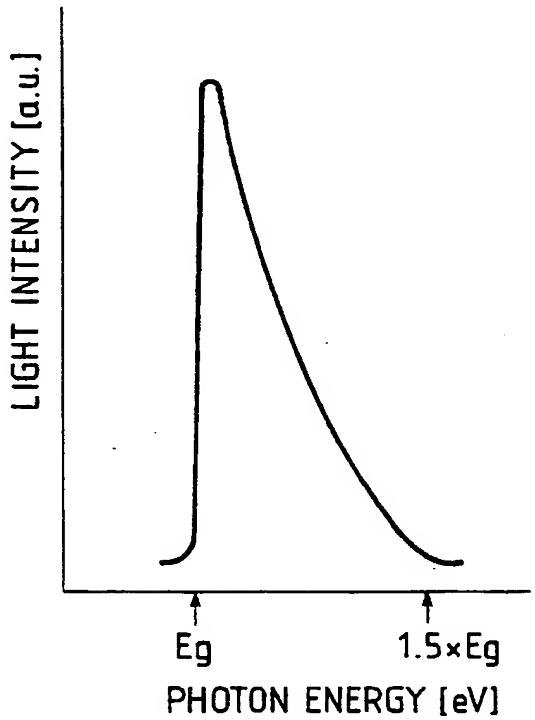

LIGHT INTENSITY [a.u.]
Eg
1.5×Eg
PHOTON ENERGY [eV]

FIG. 5

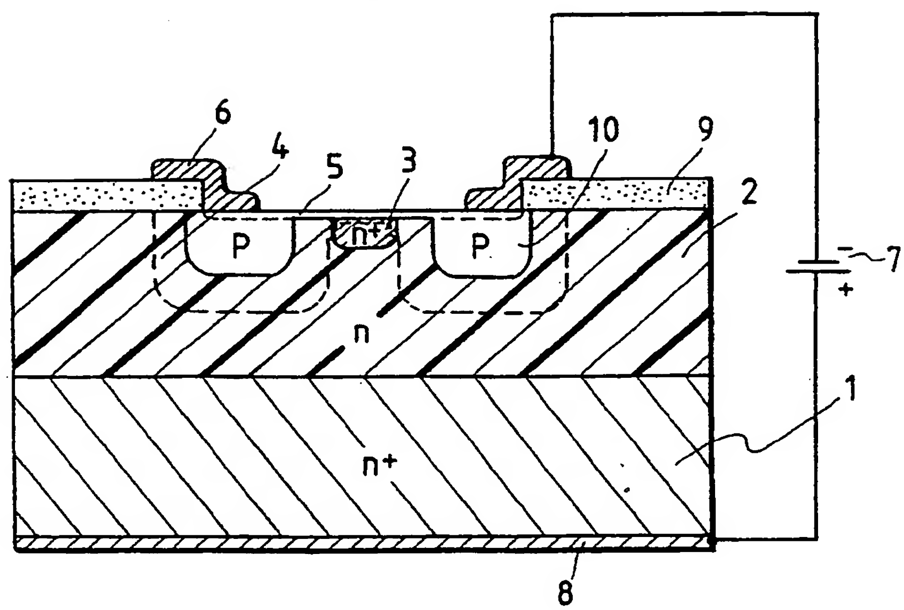

6
4
5
3
10
9
2
P
n+
P
7
n
1
n+
8

FIG. 6A

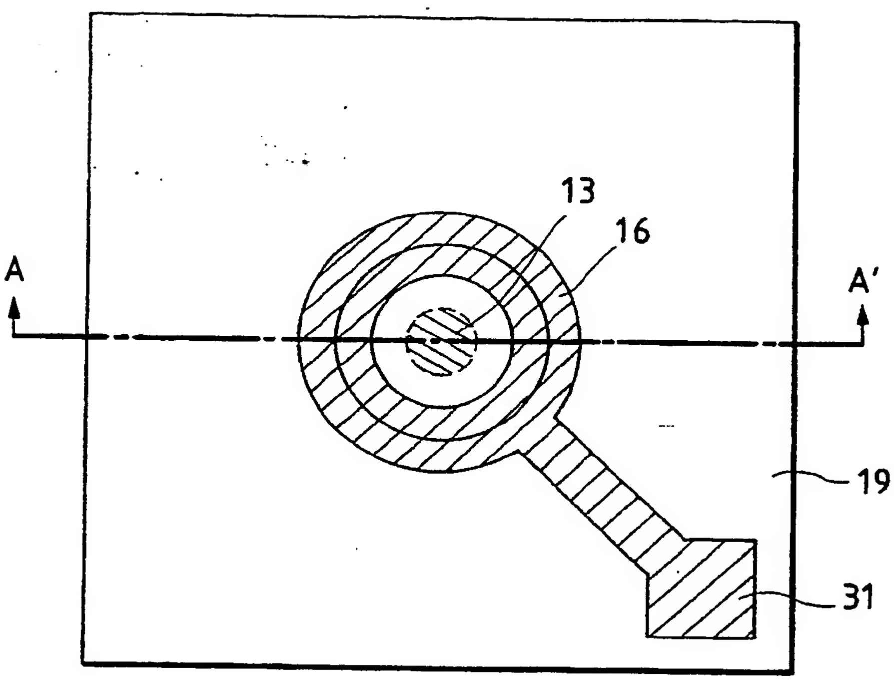


FIG. 6B

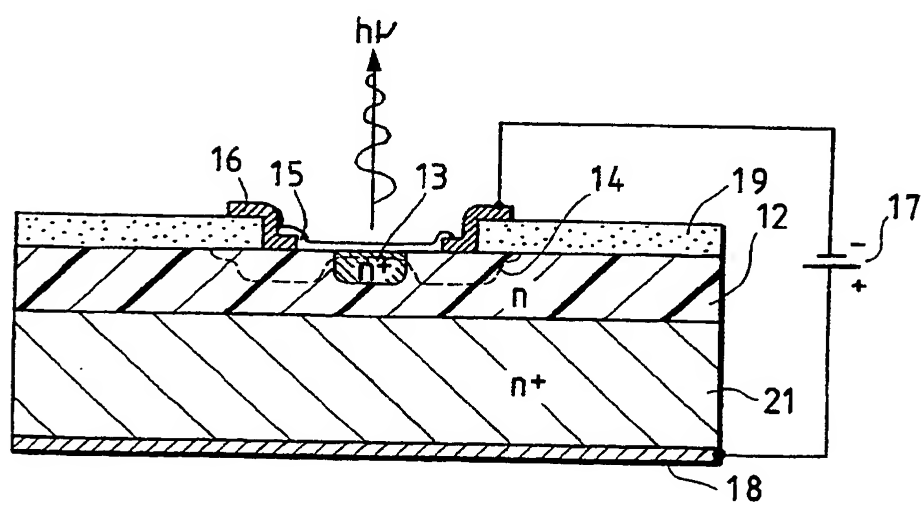


FIG. 7

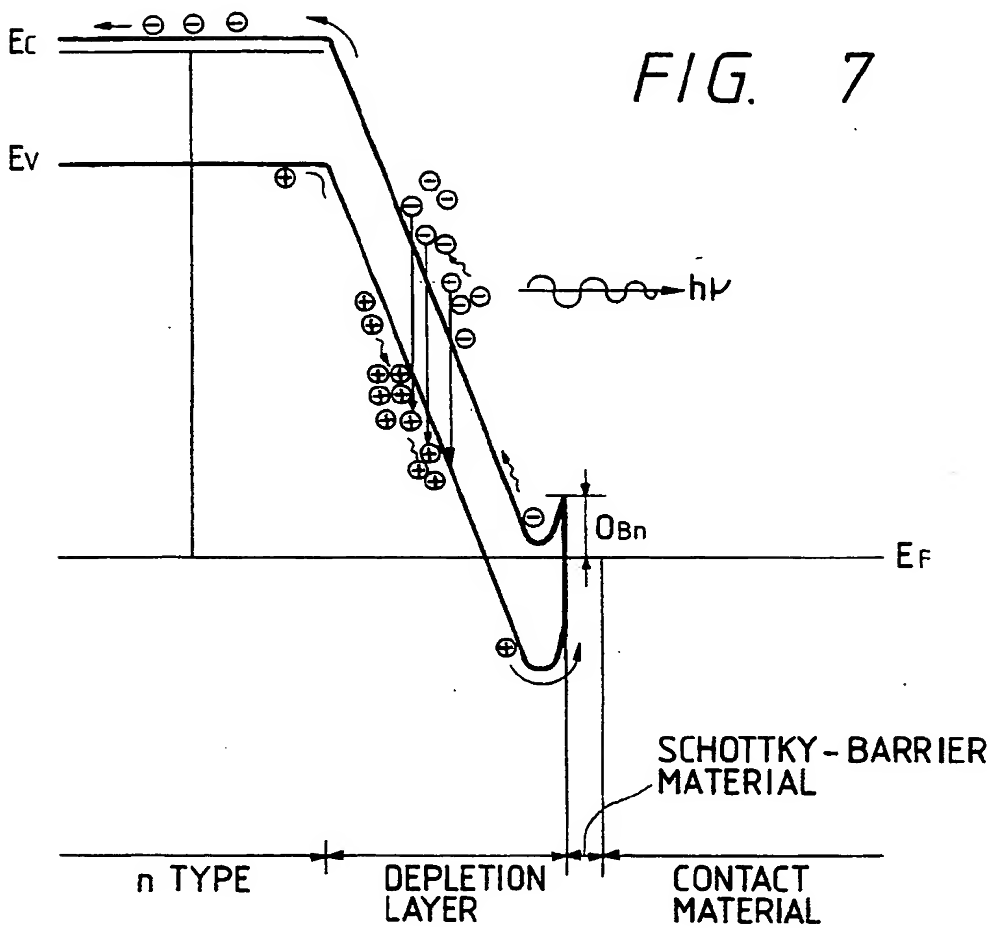
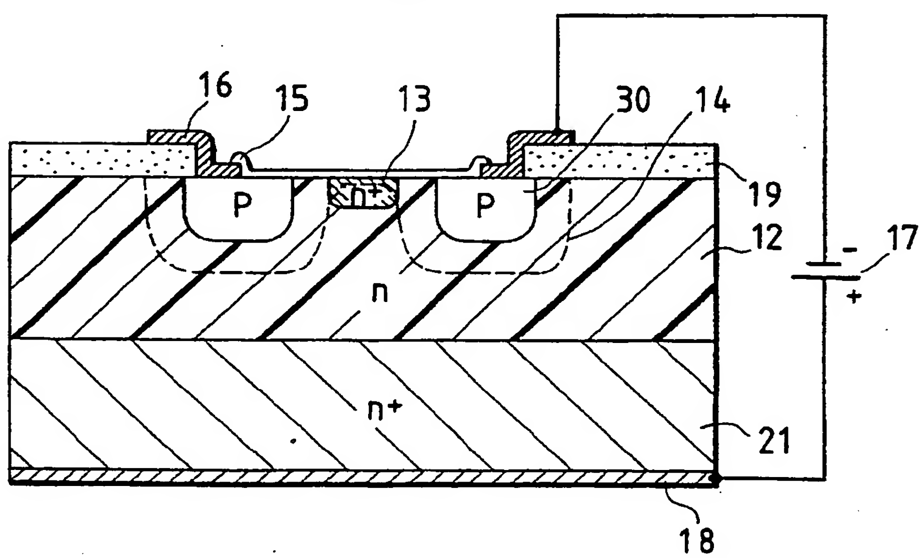

Ec
Ev
hν
ØBn
EF
SCHOTTKY-BARRIER MATERIAL
n TYPE
DEPLETION LAYER
CONTACT MATERIAL

FIG. 8


16
15
13
30
14
P
n+
P
19
12
17
n
n+
21
18

Europäisches Patentamt
European Patent Office
Office européen des brevets

(19)

(11) Publication number: **0 411 612 A3**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **90114775.1**

(51) Int. Cl.5: **H01L 33/00**

(22) Date of filing: **01.08.90**

(30) Priority: **02.08.89 JP 200481/89**
04.08.89 JP 203055/89

(43) Date of publication of application:
06.02.91 Bulletin 91/06

(84) Designated Contracting States:
DE FR GB

(88) Date of deferred publication of the search report:
11.09.91 Bulletin 91/37

(71) Applicant: **CANON KABUSHIKI KAISHA**
30-2, 3-chome, Shimomaruko, Ohta-ku
Tokyo(JP)

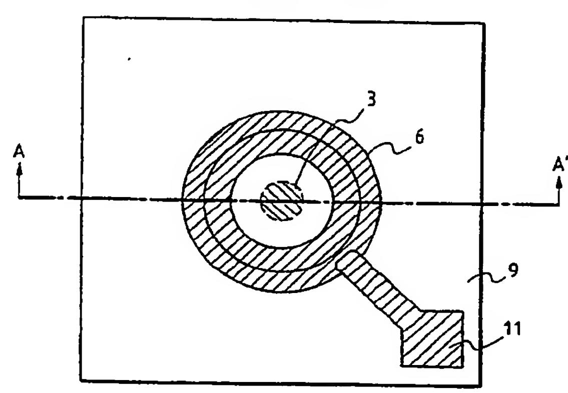
(72) Inventor: **Tsukamoto, Takeo c/o Canon Kabushiki Kaisha**
30-2, 3-chome Shimomaruko
Ohta-ku, tokyo(JP)
Inventor: **Okunuki, Masahiko, c/o Canon Kabushiki Kaisha**
30-2, 3-chome, Shimomaruko
Ohta-ku, Tokyo(JP)
Inventor: **The other inventors have agreed to waive their entitlement to designation**

(74) Representative: **Pellmann, Hans-Bernd, Dipl.-Ing. et al**
Patentanwaltsbüro
Tiedtke-Bühling-Kinne-Grupe-Pellmann-Grams-Struif Bavariaring 4
W-8000 München 2(DE)

(54) **Semiconductor light-emitting device.**

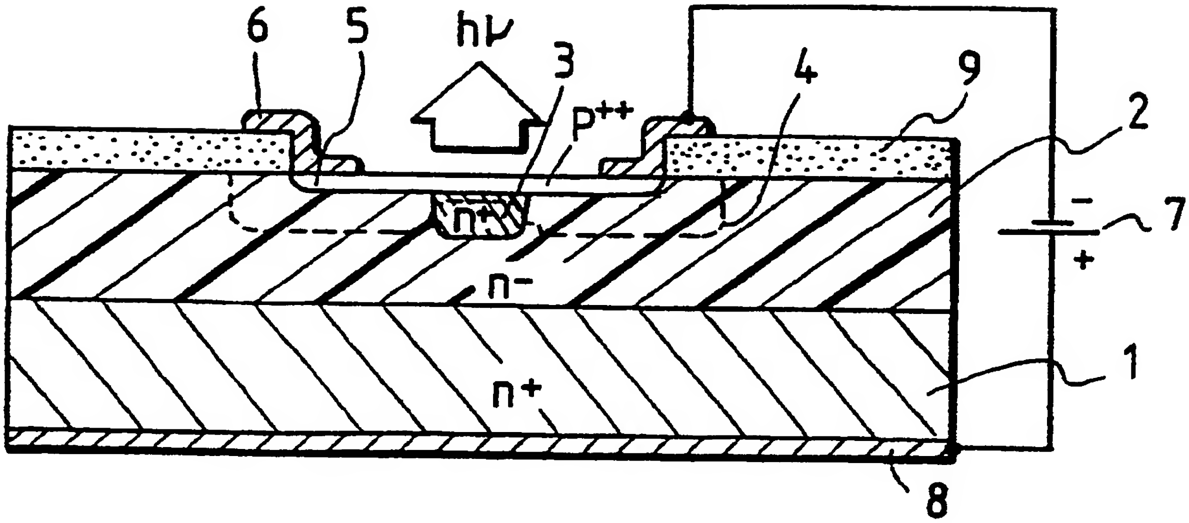
(57) A semiconductor light emitting device comprises a substrate, an n-type semiconductor layer formed on the substrate, a p-type semiconductor layer formed on a portion of a surface of the n-type semiconductor layer, an electrode for applying a reverse biasing voltage to the PN junction to cause an avalanche breakdown and an area formed in a portion of the PN junction. The p-type semiconductor layers forms a planar type PN junction with the n-type semiconductor layer. The area formed in a portion of the PN junction has a lower break down voltage than that of other area.

FIG. 1A



EP 0 411 612 A3

FIG. 1B



European Patent Office

EUROPEAN SEARCH REPORT

Application number
EP 90 11 4775

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	APPLIED PHYSICS LETTERS, vol. 55, no. 4, 24 July 1989, pages 374-376, American Institute of Physics, New York, US; J. CHEN et al.: "Photon emission from avalanche breakdown in the collector junction of GaAs/AlGaAs heterojunction bipolar transistors" * Whole article * --	1	H 01 L 33/00
A	PATENT ABSTRACTS OF JAPAN, vol. 149, no. 8 (E-255), 12 July 1984; & JP-A-59 055 085 (FUJITSU K.K.) 29-03-1984 * Whole abstract * --	1	
X,P	EP-A-0 359 329 (N.V. PHILIPS GLOEILAMPENFABRIK) * Column 2, line 18 - column 3, line 16; column 8, line 6 - column 9, line 9; figure 11 * --	1-5	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 01 L
A	EP-A-0 170 481 (NEC CORPORATION) * Page 4, line 12 - page 6, line 21; figure 1 * --	6,7	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 30, no. 6, November 1987, pages 398-399, Armonk, NY, US; "Light-emitting device" * Whole article * -- ./.	6	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13-06-1991	LINA F.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

European Patent Office

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- [ ] All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.
- [ ] Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid,

  namely claims:
- [ ] No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions,
namely:

1. Claims 1-5: Semiconductor light emitting device comprising a planar type PN junction.
2. Claims 6-10: Semiconductor light emitting device comprising a Schottky junction.

- [x] All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- [ ] Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid,

  namely claims:
- [ ] None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims,

  namely claims:

European Patent Office

EUROPEAN SEARCH REPORT

Application number
EP 90 11 4775
-2-

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	SOLID-STATE ELECTRONICS, vol. 28, no. 9, September 1985, pages 847-854, New York, US; F.J. BRYANT et al. "Blue electroluminescence in reverse-biased ZnS(Zn,Al) diodes" * Whole article *	6	

			TECHNICAL FIELDS SEARCHED (Int. Cl.5)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13-06-1991	LINA F.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO Form 1503 03 82